Fermilab Silicon Strip Readout Chip for BTEV

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Abstract— A chip has been developed for reading out the silicon strip detectors in the new BTEV colliding beam experiment at Fermilab. The chip has been designed in a 0.25 μ CMOS technology for high radiation tolerance. Numerous programmable features have been added to the chip, such as setup for operation at different beam crossing intervals. A full size chip has been fabricated and successfully tested. The design philosophy, circuit features, and test results are presented in this paper.

I. INTRODUCTION

A new colliding beams experiment called BTEV is being designed at Fermilab. The detector, which is expected to be operational in 2009, is shown in Fig. 1.
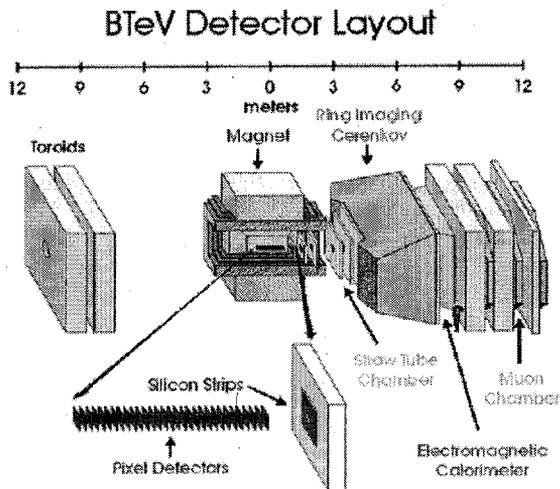
BTeV Detector Layout

Fig. 1. Overview of the BTEV detector

A major component of the detector is the silicon strip detector. The silicon strip detector planes, shown in Fig. 2, have a hole in the center for the proton and antiproton beams to pass

through. There are 7 stations of silicon strip planes with each station containing 3 planes arranged in an X, U, V orientation for a total of 129,000 silicon strip channels in the BTEV detector. Each channel requires readout electronics to measure the hit information from each strip. A full custom integrated circuit called the FSSR (Fermilab Silicon Strip Readout) chip has been designed in the TSMC 0.25 μ CMOS process to interface with the silicon strip detectors and send digital information to the data acquisition system. The FSSR chips are mounted in the area called FE electronics shown in Fig. 2.
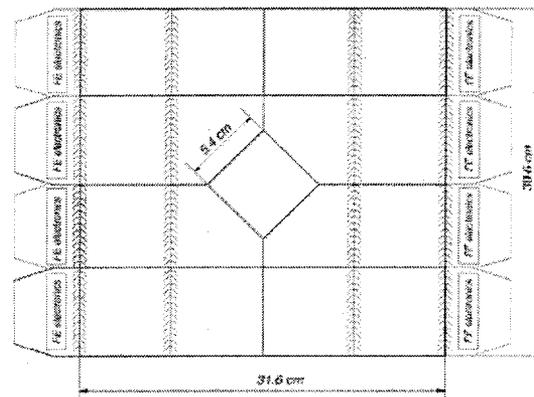

Fig. 2. One plane of silicon strip detectors showing wire bonds between detector chips and wire bonds to the Front-end electronics, where the FSSR chips are located.

Hit information from the FSSRs is used to reconstruct vertices, extrapolate tracks from the pixel detector, propagate tracks through the RICH detector to the EM calorimeter, and to control background tracks from secondary interactions.

II. FSSR DESIGN

A. General Considerations and Specifications

The FSSR chip is intended for use in a fast, data driven readout architecture. There is no trigger input to the chip and the chip has no analog storage. The chip was designed to run with a 132 nsec beam interaction rate with readout efficiencies greater than 99% at luminosity equal to 2 x 10^{32}cm^{-2}s^{-1}. Over the 10-year lifetime of the experiment, the FSSR chip is expected to see a total radiation dose of between 1 and 5 Megarads. To meet the radiation tolerance, the FSSR chip uses enclosed geometry transistors [1]. Specially designed registers are used to mitigate SEU effects. The ENC (Equivalent Noise

Charge) at the input should be less than 1000 e⁻ rms with a 20 pF detector capacitance, and the threshold dispersion across the chip should be less than 500 e⁻ rms in order to keep the noise hit rate low at a nominal 0.2 MIP (Minimum Ionizing Particle) threshold setting. Although not a major concern in this application, the power dissipation should be held to less than 4 mW/channel. Sufficient track resolution is achieved with 100 micrometer pitch silicon strip detectors and a binary readout in the FSSR. However, a low resolution ADC would be a desirable added feature to monitor detector performance with radiation. The digital readout and control of the FSSR chip was chosen to be very similar to the approach used in the pixel portion of the BTEV detector [2]. By using a common approach for the two detector subsystems, a common data acquisition system can be used.

B. FSSR Overall Design

The FSSR chip can be considered as comprised of several parts as shown in Fig. 3. The first part is the core circuitry, which includes 128 channels of analog electronics, sixteen sets of control logic (one set for every 8 input channels), and core logic, which communicates with the data interface and the rest of the core circuitry. The second part is the Programming Interface (PI) and associated registers and DACs. The PI accepts data and commands from a serial input bus and returns information upon request. Information from the PI is stored in programmable registers, which control DACs and program the chip. The third part is the Data Output Interface, which accepts data from the core, formats the data, and transmits it off the chip.
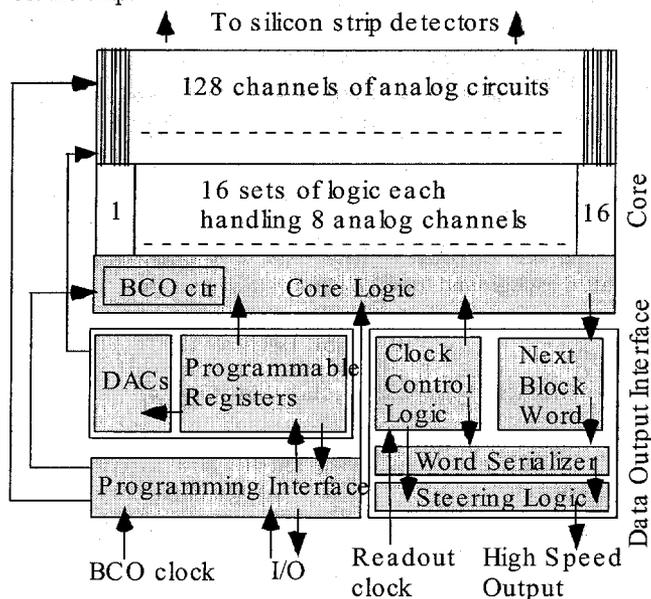

Fig. 3. Block diagram of FSSR chip showing the Core circuitry and the Data Output Interface.

Every time a strip is hit, the set number and channel number within the set is read out along with the BCO number, which is

stored in the Core Logic. The FSSR chip described in this paper was laid out with space for 128 channels. Because this was the first FSSR chip fabricated, numerous probe points were added to allow detailed testing of the chip. Alternative circuits were also included in some areas so various options could be evaluated for better performance in the final submission [3].

C. Analog Section

The analog front-end circuitry, which is replicated for every channel, is shown in Fig. 4. The major blocks are the preamplifier, integrator/shaper, BLR (base line restorer), and discriminator. 128 bit programmable shift registers are used to kill the outputs from any or all channels, and to control test input signals to each channel.
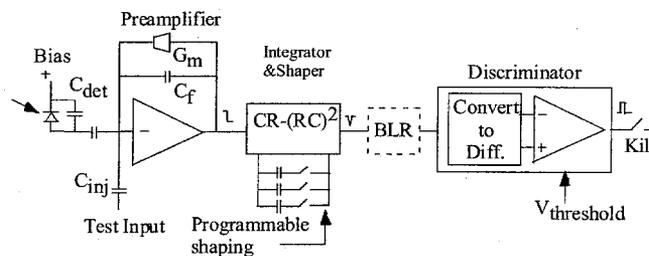

Fig. 4. Analog input section of FSSR chip.

The FSSR may have to function with beam crossing times from 132 nsec to 396 nsec, so the shaping characteristics are programmable by connecting different capacitors to the integrator and shaper. Four different shaping times (65, 85, 105, 125 nsec) are available.

At the time the chip was submitted, it was not clear whether a BLR would be necessary. The BLR, shown in Fig. 5, has the effect of changing the relative weighting of the threshold mismatch and equivalent input noise as well as changing the overall gain of the circuit. The BLR is discussed more in the results section.
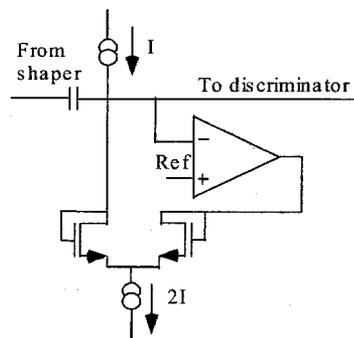

Fig. 5. Baseline restorer in the FSSR chip.

To allow for a comprehensive evaluation of noise and threshold mismatch, a number of the 128 channels were laid

out without the BLR. Thus, the block diagram in Fig. 4 shows the BLR in a dashed box. Three other design decisions were made to allow for more extensive testing of the FSSR front end. First, seven different size NMOS transistors and one PMOS transistor were used as input transistors on different channels to permit detailed noise measurements with different front-end designs. Second, for testing purposes, a small number of analog circuits were replaced with numerous probe points connected to adjacent channels, each channel having slightly different characteristics. And finally, a number of test transistors were added specifically to perform single transistor noise analysis for comparison to overall circuit performance.

D. Digital Section

The Programming Interface, Program Registers, and DACs are used to setup the chip and provide various control functions. Through the programming interface, all chips receive a serial string of bits, which includes 5 bits for chip ID, 5 bits for programmable register address, and 3 bits for instructions. Each chip has its chip ID set locally by means of 5 internal wire bonds. Information can be downloaded to one specific chip using the chip ID or all chips simultaneously using a wild chip ID address. There are 7 programmable registers:

CapSel is a 2 bit register used to set the desired shaping time in the analog section.

Kill is a 128 bit register used to disconnect the output of various discriminators in the analog section from the Core Logic.

Inject is a 128 bit register used to close a switch connecting various channels to an input pulse.

AqBCO (Acquire Beam Crossing) is an 8 bit register, which is used to hold the current value of the BCO counter in the FSSR. (The BCO counters in all FSSR chips are reset at the same time. Thus, system synchronization can be checked by loading the **AqBCO** register, reading it out later, and comparing results from all chips in the system.)

Alines is a 2 bit register used to set the number of serial output lines to 1, 2, 4 or 6.

SendData is a 1 bit register used to disable the core readout.

RejectHits is a 1 bit register used to inhibit the core from accepting any new hit information.

There are 3 other register addresses that are used for various types of resets but no information is stored.

The **CapSel**, **AqBCO**, **Alines**, **SendData**, and **RejectHits** registers have shadow registers and can be read out non-destructively at any time. The **Kill** and **Inject** registers do not have shadow registers. However, when they are read out, their contents are shifted back into the register input so that upon completion of read out, the data has been restored.

There are five instructions that can be executed for a given register address:

Write is used to download 2, 8, or 128 bits of information.
Read is used to read back information stored in a register.
Set is used to set all bits in a register = 1.
Reset is used to set all bits in a register = 0.

Default is used to set a register to its default value.

The FSSR has a data push type of readout architecture, which has been described elsewhere [2]. Data is output serially from the FSSR using LVDS. One feature of the Data Output Interface is the ability to program the number of serial output lines to be used depending on the expected hit activity in a given chip. A chip with low activity can use just one output serial pair while a chip in a very active area may have as many as 6 output pairs transmitting data off the chip. This means that no buffering of the output data is required on the chip. The Data Output Interface formats the information to be transmitted and adjusts the internal clocking frequencies so that all hit data in a single BCO is normally read out in about 1 BCO time interval.

The BCO clock may be either 3.78 MHz or 2.52 MHz. The FSSR readout clock is designed to be 70 MHz, and not tied to the BCO clock. Information is read out on both edges of the readout clock for a maximum data transmission rate of 840 Mb/sec. Status/Sync information and hit information are read out at different times depending on the hit activity in the chip. A readout word is comprised of 24 bits. The status/sync word has 10 bits of status, 13 bits for synchronization, and 1 bit for a word mark. The data word has 8 bits for the BCO number associated with the hit, 5 bits for the number of the logic set handling the hit, 4 bits for the number of the hit silicon strip, and 1 bit for a word mark (6 bits are currently unused). Data sent from the chip is not time ordered. The BCO number is used off line to reconstruct beam interactions. Since point-to-point communication is used, no chip ID information is needed in the data output.

The output data bit format changes when different numbers of output pairs are used. As mentioned, an output word is 24 bits long (b0 to b23). Fig. 6 shows how the bits are ordered for 1, 2, 4 or 6 output lines.
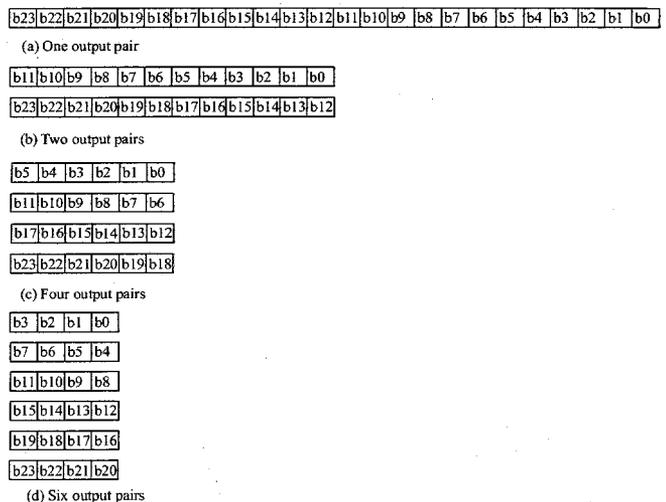

Fig. 6. Output data format with (a) one output pair, (b) two output pairs, (c) four output pairs, (d) six output pairs.

III. TEST RESULTS

The analog channels in the FSSR were laid out on a 50 μ pitch with input bonding pads arranged in two rows having an effective pitch of 50 μ. Fig. 7 is a photo of the FSSR chip.
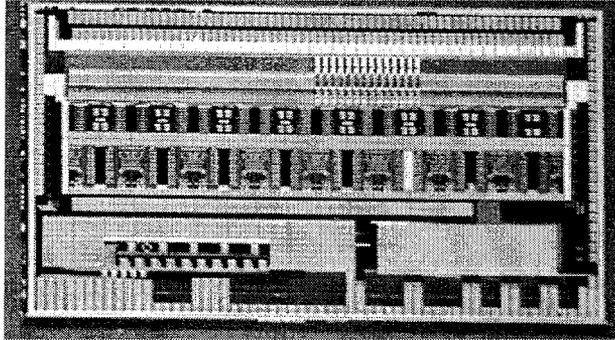

Fig. 7. FSSR chip with input pads at the top and outputs at the bottom.

The FSSR has been successfully tested as a stand-alone chip and with strip detectors. Both the analog and digital sections along with all the test structures have functioned properly, allowing extensive testing of the chip to be completed.

Tests were performed on individual NMOS and PMOS transistors, which showed that, as expected, NMOS devices would have superior noise performance over PMOS devices in the preamplifier input. This was confirmed on measurements of analog channels with different input devices. Tests on channels with gate lengths of 0.35 μ, 0.45 μ, and 0.55 μ showed that best noise performance is achieved when L= 0.45 μ or greater. Similar measurements were made with W = 1000 μ, 1500 μ, and 2000 μ using different shaping times. For low noise, the optimal size for the input transistor was found to be about W/L=1500μ/0.45μ.

The shaping time of the FSSR is easily adjustable by changing capacitors in the integrator and shaper. Four values
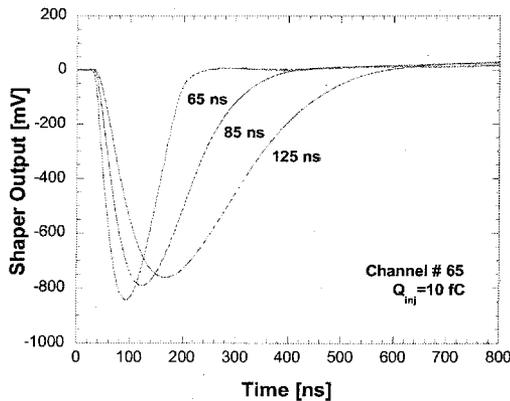

Fig. 8. Averaged waveforms at shaper output showing different shaping time settings.

of shaping time can be set ranging from 65 nsec to 125 nsec. This range allows for good operation with foundry process variations and different beam interaction times. Shaper output signals for three different settings are shown in Fig. 8.

The FSSR analog front end is well behaved for large and small input signals as shown in Fig. 9. The gain of the preamplifier is set by the preamplifier feedback capacitor (200 fF) to be 5 mV/fC. The overall gain of the preamplifier, integrator and shaper is about 80 mV/fC as seen in Figs. 8 and 9.
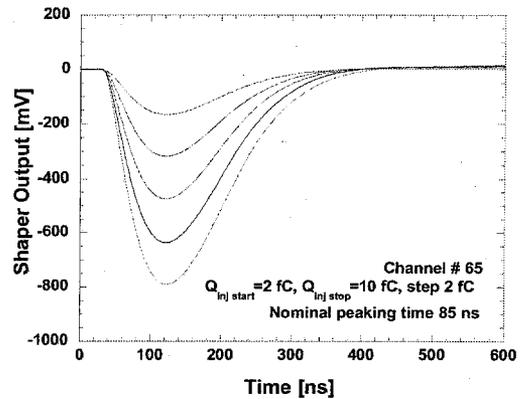

Fig. 9. Averaged waveforms at the shaper output for different input charges.

In general, the performance of the analog section is in good agreement with early simulations. Noise measurements were close to expected values. Figure 10 shows a typical noise plot.
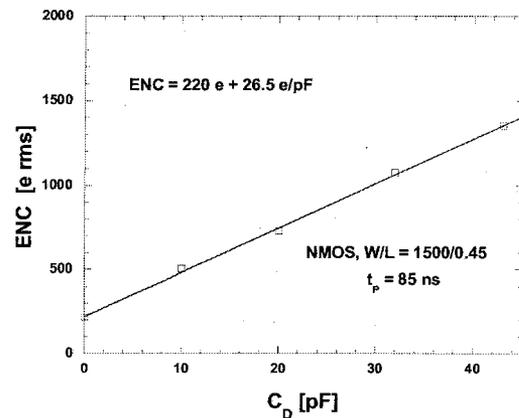

Fig. 10. Noise measurement at shaper output for medium speed shaping time, and a typical input transistor.

A major feature to be evaluated in the FSSR chip was the need and performance of the BLR. One block of 64 channels was designed and laid out with 32 channels having a BLR and 32 without. The normal response from the shaper circuit has a small overshoot, which lasts for several microseconds. The result is a variable baseline shift at the shaper output that affects the threshold level in the discriminator. To verify simulations, a test was performed where a 4 fC signal was

injected repeatedly to create a baseline shift before the arrival of a test signal. The test signal was used to construct a threshold scan in the discriminator to measure threshold shifts in the discriminator. Results showing the change in threshold for low occupancy (without baseline shift) and 1% and 2% occupancy are shown in Fig. 11. The expected occupancy in some but not all parts of the detector was found to cause a significant threshold shift. Fig. 12 shows a similar test with a BLR at the shaper output where the presence of the baseline shift has been removed.
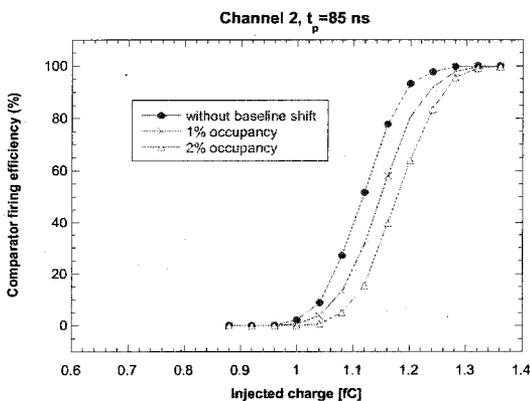

Fig. 11. Effective change in discriminator threshold due to shaper response at 0%, 1%, and 2% occupancy, without the presence of a BLR.
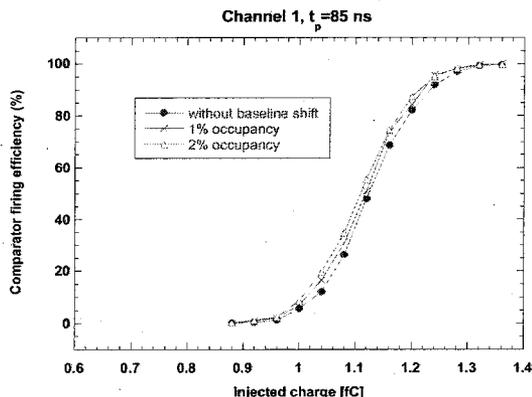

Fig. 12. Effective change in discriminator threshold due to shaper response at 0%, 1% and 2% occupancy with a BLR.

The addition of a BLR has a profound effect on the gain, noise, and threshold dispersion of the overall circuit. Since the BLR is AC coupled to the shaper, the overall threshold dispersion, due to the shaper, is reduced by adding the BLR. However, the presence of the BLR itself increases the overall ENC of the circuit. Both the threshold dispersion and noise must be considered together to obtain optimal performance. Introduction of the BLR circuit also reduces the overall gain by 20%.

Table 1 shows approximate noise and threshold dispersion for a circuit with and without a BLR for $C_{det} = 20$ pF. After analysis, it has been determined that the BLR circuit is needed.

	Threshold Dispersion	ENC
W/O BLR	790 erms	760 erms
W BLR	440 erms	890 erms
Specification	500 erms	1000 erms

Table 1. Typical threshold dispersion and equivalent noise charge with and without a Base Line Restorer circuit for a shaping time of 85 nsec.

IV. FUTURE CHANGES

The current FSSR design has an unnecessarily wide dynamic range. On the final version of the FSSR, the gain will be increased by decreasing the size of the preamplifier feedback capacitor from 200 fF to 150 or 100 fF. This will result in a further reduction in threshold dispersion. Simulations have shown the smaller capacitor value to be acceptable in terms of dynamic range and stability.

Although a simple binary output is sufficient for track reconstruction, it has been recently decided that a simple binary readout system will not satisfy the need to calibrate the detector as radiation changes its characteristics. In order to have an absolute calibration of the system with the present design, the MIP peak would have to be measured by a suitable threshold scan on all channels. This would be very time consuming. A better approach would be to have a 3-bit ADC on every channel. Since a 3-bit FADC design has already been implemented on the BTEV FPIX2 chip [2], it has been decided to add a similar ADC to the FSSR. The three bits of data from each strip will replace three of the six unused bits in the data word output stream. Thus there is no change in the overall readout speed. The above changes and other smaller changes will be completed for submission of a pre-production chip by early 2005.

V. CONCLUSION

A full size FSSR chip has been designed and tested. The device was fully functional. Tests showed that the BLR circuit was necessary. With the BLR, all initial requirements were met. The final design will include a 3 bit FADC to permit better calibration of the detector. The next version is expected to be the pre-production device.

VI. REFERENCES

[1] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, et al., "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1690-1695, Dec. 1997.

[2] J. Hoff, A. Mekkaoui, D. Christian, S. Zimmerman, G. Cancelo, P. Kasper, R. Yarema, "PreFPIX2: Core Architecture and Results," *IEEE Trans. Nucl. Sci*, vol. 48, no. 3, pp. 485-492, June 2001.

[3] Pier Francesco Manfredi, Massimo Manghisoni, Lodovico Ratti, Valerio Re, Valeria Speziali, Luigi Moroni, Jim Hoff, Abderrezak Mekkaoui, Raymond Yarema, David Christian, Simon Kwan, "The Fermilab Silicon Strip Readout Test Chip," BTEV-doc-2866-v1, March 30, 2004.